



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,842	09/28/2006	Masahiro Murakawa	KUB-006	3715
32628	7590	07/23/2008	EXAMINER	
KANESAKA BERNER AND PARTNERS LLP			GARBOWSKI, LEIGH M	
1700 DIAGONAL RD				
SUITE 310			ART UNIT	PAPER NUMBER
ALEXANDRIA, VA 22314-2848			2825	
			MAIL DATE	DELIVERY MODE
			07/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,842	MURAKAWA ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 28 September 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-8 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-8 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 28 September 2006 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>05/04/2007</u> . | 6) <input type="checkbox"/> Other: _____ . |

Specification

The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code [page 2, line 25]. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1 and 8 are rejected under 35 U.S.C. 112, first paragraph, as a single means claim(s). The claims merely comprise a parameter adjusting means, not in combination with another recited element of means, resulting in undue breadth. See MPEP 2164.08(a).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 6 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. A “program” is not statutory subject matter; a computer program per se does not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program’s functionality to be realized. A computer program is merely a set of instructions capable of being executed by a computer, the computer program itself is not a process. A computer-readable medium is needed to realize the computer program’s functionality. When a computer program is claimed in a process where the computer is executing the computer program’s instructions, the claim is treated as a process claim. Therefore, the claim is rejected for being directed to non-statutory functional descriptive material.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen, Cheng-Kai ["A Genetic Algorithm for Deep-Submicron MOSFET Parameters Extraction and Simulation"].

As per claim 1, a parameter adjusting device comprising parameter adjusting means adopting a surface potential model wherein a formula for analysis is derived based on surface potential as a circuit design model of a semiconductor element; defining a chromosome with genes as a respective great number of parameters of the circuit design model of the semiconductor element; and optimizing said parameters using a genetic algorithm based on property measured data of the tested semiconductor element [Abstract; section 2.1.1; Chapter 3]. As per claim 2, wherein said parameter adjusting means comprises: first portion parameter adjusting means at least adjusting the parameters which determine the structure of the semiconductor element based on the property measured data of the semiconductor element belonging to a long channel group [sections 2.1.1, 2.2, 4.2, 4.4; Chapter 3]; and second portion parameter adjusting means at least adjusting the parameters which require adjustment, excepting the parameters being adjusted by said first portion parameter adjusting means based on the property measured data of various length of channels, with reference to an adjustment result of said first portion parameter adjusting means [sections 2.1.1, 2.2, 4.2, 4.4; Chapter 3]. As per claim 3, wherein said parameter adjusting means adopts HiSIM as said surface potential model, and comprising: said first portion parameter adjusting means adjusting a part of the parameters of a technological parameter group of the HiSIM, and a part of the parameters which is determined by the determination of technological parameters of a mobility parameter group [sections 2.1.1, 2.2, 4.2, 4.4, 5.2; Chapter 3;]; and said

second portion parameter adjusting means also readjusting a part of the parameters being adjusted by said first portion parameter adjusting means [sections 2.1.1, 2.2, 4.2, 4.4, 5.2; Chapter 3]. As per claim 4, wherein said portion parameter adjusting means comprises generating range determination means obtaining the center of gravity in the vector space of a parent chromosome group, in crossover processing of a genetic algorithm, and determining a generating range of a child chromosome group inside a hyperpolyhedron in the vector space which is determined by values of said center of gravity and parent chromosome group [Chapter 3]. As per claim 5, wherein said portion parameter adjusting means comprises: evaluated value calculation means obtaining both the first evaluated value based on the data of a linear scale and the second evaluated value based on the data of a log scale, in selection processing of the genetic algorithm, and determining a total of the first evaluated value and the second evaluated value as the evaluated value of said chromosomes [Chapter 3]; and normalization means unifying a scale of the data [Chapter 3].

As per claim 7, a parameter adjusting method in a surface potential model wherein a formula for an analysis is derived based on a surface potential as a circuit design model of a semiconductor element, comprising: a first step defining chromosomes wherein great number of parameters of the circuit design model of the semiconductor element are the genes, and adjusting the parameters which determine the structure of the semiconductor element using a genetic algorithm based on property measured data of a long channel group of the tested semiconductor element [sections 2.1.1, 2.2, 4.2, 4.4; Chapter 3]; and a second step defining chromosomes wherein the respective great number of parameters of the circuit design model of the semiconductor element are the genes, and adjusting the parameters which are required to be adjusted, excepting the parameters adjusted in at least said first step, using a genetic algorithm, based on the property measured data of various length of channels of the tested semiconductor element, with reference to an adjustment result of said first step [sections 2.1.1, 2.2, 4.2, 4.4; Chapter 3].

As per claim 8, a parameter adjusting device comprising parameter adjusting means which adapts an electric charge model wherein a formula for an analysis is derived based on an electric charge as a circuit design model of a semiconductor element; defines chromosomes wherein great number of parameters of a circuit design model of the semiconductor element are the genes; and optimizes said parameters based on the property measured data of a tested semiconductor element, using a genetic algorithm [Abstract; section 2.1.1; Chapter 3].

Claims 1, 4-5 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by KESER, Milan and JOARDAR, Kuntal ["Genetic Algorithm Based MOSFET Model Parameter Extraction"].

As per claim 1, a parameter adjusting device comprising parameter adjusting means adopting a surface potential model wherein a formula for analysis is derived based on surface potential as a circuit design model of a semiconductor element; defining a chromosome with genes as a respective great number of parameters of the circuit design model of the semiconductor element; and optimizing said parameters using a genetic algorithm based on property measured data of the tested semiconductor element [sections 2 and 3]. As per claim 4, wherein said portion parameter adjusting means comprises generating range determination means obtaining the center of gravity in the vector space of a parent chromosome group, in crossover processing of a genetic algorithm, and determining a generating range of a child chromosome group inside a hyperpolyhedron in the vector space which is determined by values of said center of gravity and parent chromosome group [sections 3 and 4]. As per claim 5, wherein said portion parameter adjusting means comprises: evaluated value calculation means obtaining both the first evaluated value based on the data of a linear scale and the second evaluated value based on the data of a log scale, in selection processing of the genetic algorithm, and determining a total of the first evaluated value and the second evaluated value as the evaluated value of said chromosomes [sections 3 and 4]; and normalization means unifying a scale of the data [sections 3 and 4].

As per claim 8, a parameter adjusting device comprising parameter adjusting means which adapts an electric charge model wherein a formula for an analysis is derived based on an electric charge as a circuit design model of a semiconductor element; defines chromosomes wherein great number of parameters of a circuit design model of the semiconductor element are the genes; and optimizes said parameters based on the property measured data of a tested semiconductor element, using a genetic algorithm [sections 2 and 3].

Claims 1-2, 4-5 and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Bittner et al. [U.S. Patent #6,314,390 B1].

As per claim 1, a parameter adjusting device comprising parameter adjusting means adopting a surface potential model wherein a formula for analysis is derived based on surface potential as a circuit design model of a semiconductor element; defining a chromosome with genes as a respective great number of parameters of the circuit design model of the semiconductor element; and optimizing said parameters using a genetic algorithm based on property measured data of the tested semiconductor element [column 5, lines 6-14, 33-59; column 6, lines 12-41]. As per claim 2, wherein said parameter adjusting means comprises: first portion parameter adjusting means at least adjusting the parameters which determine the structure of the semiconductor element based on the property measured data of the semiconductor element belonging to a long channel group [column 5, lines 6-14, 33-59; column 6, lines 12-41]; and second portion parameter adjusting means at least adjusting the parameters which require adjustment, excepting the parameters being adjusted by said first portion parameter adjusting means based on the property measured data of various length of channels, with reference to an adjustment result of said first parameter adjusting means [column 5, lines 6-14, 33-59; column 6, lines 12-41]. As per claim 4, wherein said portion parameter adjusting means comprises generating range determination means obtaining the center of gravity in the vector space of a parent chromosome group, in crossover processing of a genetic algorithm, and determining a generating range of a child chromosome group inside a hyperpolyhedron in the vector space which is

determined by values of said center of gravity and parent chromosome group [column 5, lines 33-59; column 6, lines 12-41]. As per claim 5, wherein said portion parameter adjusting means comprises: evaluated value calculation means obtaining both the first evaluated value based on the data of a linear scale and the second evaluated value based on the data of a log scale, in selection processing of the genetic algorithm, and determining a total of the first evaluated value and the second evaluated value as the evaluated value of said chromosomes [column 5, lines 33-59; column 6, lines 12-41]; and normalization means unifying a scale of the data [column 5, lines 33-59; column 6, lines 12-41].

As per claim 7, a parameter adjusting method in a surface potential model wherein a formula for an analysis is derived based on a surface potential as a circuit design model of a semiconductor element, comprising: a first step defining chromosomes wherein great number of parameters of the circuit design model of the semiconductor element are the genes, and adjusting the parameters which determine the structure of the semiconductor element using a genetic algorithm based on property measured data of a long channel group of the tested semiconductor element [column 5, lines 6-14, 33-59; column 6, lines 12-41]; and a second step defining chromosomes wherein the respective great number of parameters of the circuit design model of the semiconductor element are the genes, and adjusting the parameters which are required to be adjusted, excepting the parameters adjusted in at least said first step, using a genetic algorithm, based on the property measured data of various length of channels of the tested semiconductor element, with reference to an adjustment result of said first step [column 5, lines 6-14, 33-59; column 6, lines 12-41].

As per claim 8, a parameter adjusting device comprising parameter adjusting means which adapts an electric charge model wherein a formula for an analysis is derived based on an electric charge as a circuit design model of a semiconductor element; defines chromosomes wherein great number of parameters of a circuit design model of the semiconductor element are the genes; and optimizes said parameters

based on the property measured data of a tested semiconductor element, using a genetic algorithm [column 5, lines 6-14, 33-59; column 6, lines 12-41].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. COELLO, Carlos A. discloses "An Updated Survey of GA-Based Multiobjective Optimization Techniques." Higuchi et al. [U.S. Patent #6,637,008 B1] disclose adjusting using a genetic algorithm.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893. The examiner can normally be reached on days. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leigh Marie Garbowski/
Primary Examiner, Art Unit 2825